UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/775,254	02/11/2004	Hiroshi Iwata	0397-0475P	9897

2292 7590 11/22/2005

BIRCH STEWART KOLASCH & BIRCH
PO BOX 747
FALLS CHURCH, VA 22040-0747

EXAMINER	
NGUYEN, TAN	

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 11/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/775,254	IWATA ET AL.	
	Examiner	Art Unit	
	Tan T. Nguyen	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 November 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *10-22* is/are allowed.

6)☒ Claim(s) *1-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. The following action is in response to the amendment filed by Applicants on November 8, 2005.

2. The Terminal Disclaimer submitted by Applicants on November 8, 2005 has been received.

3. The Information Disclosure Statement submitted by Applicants on October 6, 2005 has been received and fully considered.

4. Claims 1-22 are pending.

5. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., In re Berg, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); In re Goodman, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); In re Longi, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); In re Van Ornum, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); In re Vogel, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and In re Thorington, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

6. Claims 1-9 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1, 7-9 of U.S Patent application No. 10/808,581 (hereinafter U.S. Pat. Application '581), claims 1, 11-13 of U.S. Patent Application No. 10/505,433 (hereinafter U.S. Pat. Application No. '433),

claims 1, 9-13 of U.S. Patent application No. 10/506,322 (hereinafter U.S. Pat. Application No. '322), and claim 1 of copending Application No. 10/513,959 (hereinafter U.S. Pat. Application No. '959). Although the conflicting claims are not identical, they are not patentably distinct from each other because the claims of the copending applications recited similar limitations of claims 1-9 of the present application.

Regarding claim 1 of the present application, claims 1 of U.S. Pat. Application No. '433, No. '322, No. 959 and No. '581 recited a semiconductor storage device comprising a semiconductor substrate, a gate insulating film formed on the semiconductor substrate, a single gate electrode formed on the gate insulating film, two charge holding portions (memory function parts) formed on opposite sides of the single gate electrode, channel region disposed under the single gate electrode, diffusion layer regions of second conductivity formed on both sides of the channel region.

Regarding claim 2 of the present application, it is inherent that column select transistors are serially connected to the memory cell in NAND string non-volatile memory.

Regarding claim 3 of the present application, claim 7 of U.S. Pat. Application No. '581, claim 11 of U.S. Pat. Application No. '433 and claim 13 of U.S. Pat. Application No. '322 recited at least part of the charge holding portion is formed so as to overlap part of the second conductivity type diffusion layer region.

Regarding claim 4 of the present application, claim 8 of U.S. Pat. Application No. '581, claim 12 of U.S. Pat. Application No. '433 and claim 11 of U.S. Pat. Application No. '322 recited each of the memory function bodies includes a film having a surface

roughly parallel to a surface of the gate insulating film and having a function of retaining electric charges.

Regarding claim 5 of the present application, claim 13 of U.S. Pat. Application No. '433 and claim 12 of U.S. Pat. Application No. '322 recited the film made of the first insulator having a function of charge storage includes a portion that extends approximately parallel to sides of the gates electrodes.

Regarding claim 6 of the present application, claim 8 of U.S. Pat. Application No. '581 and claim 9 of U.S. Pat. Application No. ' 322 recited an insulating film separating the film having the function of retaining electric charge from the channel region or the semiconductor layer, the insulation film having a film thickness of the gate insulation film and not smaller than 0.8 nm.

Regarding claim 7 of the present application, claim 10 of U.S. Pat. Application No. '322 recited the charge holding portion has structure in which a film composed of the first insulator having a function of storing electric charges is interposed between the second and the third insulator, the thickness of the film composed of the second insulator on the channel region is larger than the thickness of the gate insulating film and is 20 nm or less.

Regarding claims 8-9 of the present application, claim 9 of U.S. Pat. Application No. 581 recited portable electronic equipment, which includes the display device in claim 8 of the present application, having the semiconductor storage device in claim 1

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by Hong et al. (U.S. Patent No. 5,457,061).

Hong et al. disclosed in Figure 6 a top floating gate FLASH EEPROM comprising a substrate [30] which has been p-doped (column 3, line 26), an oxide layer [32] (column 3, line 28) which functions as an insulating layer (claim 1, line 3) formed over the substrate [30], a first polysilicon layer [34] is patterned to form word line [38] (column 3, lines 54-56), the word line [38] is known as the control gate which is understood as the claimed gate electrode, a floating gate [44] is disposed over the top and the opposite sides of the word line [38] (column 4, lines 33), the drain [50] and source regions [52] of N-type are formed by ion implantation (column 4, line 38). The region under the control gate and between the drain region [50] and source region [52] is known as the channel region.

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. ***

Amin is cited to show memory device having floating gate disposed over and on both sides of the floating gate. Sung-Mu is cited to show a memory device having floating gate disposed on both sides of the control gate.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tan T. Nguyen whose telephone number is (571) 272-1789. The examiner can normally be reached on Monday to Friday from 07:00 AM to 03:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian, can be reached at (571) 272-1852. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tan T. Nguyen
Primary Examiner
Art Unit 2827
November 17, 2005